Patent Abstract

GER 2003-02-13 10229945 **MICROPROCESSOR INTERRUPT CONTROLLER HAS MEANS FOR PROCESSING INTERRUPTS SUCH THAT REQUESTS OF LOWER PRIORITY DO NOT EXECUTE AHEAD OF HIGHER PRIORITY REQUESTS, PROVIDED THEY ARE STILL WITHIN THEIR GIVEN LATENCY TIME**

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Interrupt controller comprises parallel input (30) for receipt of a first interrupt request signal, means (31) for output of a second interrupt request signal as a reaction to the first interrupt request signal, state processing means (32) for determining interrupt priority, memory (37) for storing addresses of interrupt servicing programs whereby each servicing program handles an interrupt signal and means (36) for selection of an address based on the priority.
EXEMPLARY CLAIMS- 1. An interrupt CONTROLLER, containing: Parallel entrance means (30) to the receiving of first interruptrequest signals; Means (31, 32) to the expenditure of a second interrupt request signal as reaction to the receipt at least one of the first interrupt request signals; Condition machine means (33, 34, 35, 36) to intending a priority for each of the first interrupt request signals; Memory means (37) to storing addresses of interruption utility programs, whereby each of the interruption utility programs is assigned to one of the first interrupt request signals; Means (36) to selecting one of the addresses on the basis of the priority. 2. The interrupt CONTROLLERS in accordance with requirement 1, with which the parallel entrance means exhibit a numberof separate connection channels, whereby everyone of the separate connection channels is so laid out that it receives one of the first interrupt request signals from an external device. 3. The interrupt CONTROLLERS in accordance with requirement 1 or 2, which furthermore means exhibits for the adaptation of the interrupt and/or for the classification of the interrupt and/or to prescreeners of the interrupt. 4. The interrupt CONTROLLERS in accordance with requirement 1, 2 or 3, whereby the first interrupt request signals areelevatorsteered interrupt request signals. 5. The interrupt CONTROLLERS in accordance with one the arbitrary managing requirements 1 to 4, which furthermore means (31) exhibits for spending data, which are referring one or to severalof the first interrupt request

signals, which became to receive from the parallel entrance means as input signal for the condition machine means. 6. The interrupt CONTROLLERS in accordance with one the arbitrary managing requirements 1 to 5, in which the condition machine means exhibits a register file (35) for storing a priority foreach of the first interrupt request signals. 7. The interrupt CONTROLLERS in accordance with one the arbitrary managing requirements 1

NO-DESCRIPTORS